

## Curriculum Vita

Dr. Marwan Hassoun

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### Major Highlights

- Senior Vice President of Engineering at Keyeye Communication, Inc. Built and lead a team of 50+ Analog, DSP, Systems and Digital engineers distributed in Sacramento, Minneapolis, Florida, India and Australia to the development of industry's lowest power 10GBASE-T solution. The complex chip included 800MHz custom DSP, 1Gsps 9-bit quad ADCs, 1Gsps 10-bit DACs, 3.2GHz PLLs and an IFFT/FFT custom ultra-low power processor for Echo/Next cancellation all operating as a single system. Also drove the intellectual property strategy and over 18 patent applications generated on the technology. Was directly involved in fund raising and pursuing potential M&A opportunities.
- Sr. Director of Engineering for the Communications Technology Division at Xilinx, Inc. This includes a team of 60+ engineers in Austin, Minneapolis, San Jose and Ames. Responsible for producing the high-speed serial Multi-Gigabit Transceiver technology (622Mhz – 11.1Gbps) in the platform FPGAs (Virtex Family) programmable to support over 10 different serial technologies. The technology represented the 1<sup>st</sup> FPGAs to be introduced in the marketplace with greater than 4Gbps serial I/O technology. The challenge was producing 1<sup>st</sup> pass working silicon in extremely advanced process technologies which required developing of redundancy, calibration and error correction technology to offset the variability of the processes. Was awarded innovation of the year award in 2003. In addition, responsible for the entire product line (from design to production) of Xilinx's 1<sup>st</sup> ASSP family (RocketPHY) operating at 10.3Gbps and 10.7Gbps. There were over 50 patent applications on the different fascists of the technology. Selected to serve on Xilinx's Patent Committee.
- President & Managing Partner in TraCHip, LLC, an intellectual property company.
- Co-Founded a development stage company, MadMax Optics, INC. and guided it through the seed round funding.
- Part of establishing and managing a startup company, RocketChips, INC. from inception in 1997 till acquisition in 2000. Roles included (from 1997–1998 as early investor and technical contributions via ISU, and from 1998 till acquisition in 2000 as Senior Technical Director initially and then Vice President of Wired Products). Managed multi-company and multi-country (Japan, India and US) IC design product as well as major customers including INTEL, SONY and OKI. Major products included cutting edge high-speed serial transceiver technology ranging from 1Gbps in 1997 to 10Gbps by 2000. Products introduced included IEEE1394 transceivers (400Mbps) and programmable ADCs and DAC Intellectual Property.
- Responsible for design of several power management IC products while with Texas Instruments. This includes several of the TPS202X, TPS203X, TPS204X, TPS208X and TPS209X family members. In addition part of ASIC design team for cell-phone applications.
- 15 patents granted and 7 pending in the areas of multi-gigabit serial transceivers, high-speed high-resolution ADCs and DACs, Magnetic RAMs, RFID, DSP filters and Power

### Management.

- Over 70 technical publications in National and International Journals and Conferences.
- Co-Founded the Analog and Mixed-Signal VLSI Design Center at Iowa State University in 1996. The funding grew from \$300K in 1996 to over \$4M in 1998. Served as Director of the Center. Attracted sponsorship for the Center from major companies that include Texas Instruments, Honeywell, Rockwell, RocketChips, Non-Volatile Electronics and VTC.
- Served as Chair of the VLSI area in the Department of Electrical and Computer Engineering at Iowa State University.
- Served as expert witness cases involving major semiconductor companies.
- Established, drove, participated and negotiated Intellectual Property Strategy at all positions since 1994.

**EXPERIENCE**Mar 08 – Present

President, CEO and Founder  
**Green Semiconductor, Inc.**, Austin, TX

Founded a development stage company with the near-term goal of monetization of intellectual property: patents and high-speed design blocks, and a long-term goal of funding and building an environmentally and socially conscious high-tech Company.

Mar 03 – Present

President & Managing Partner  
**TraCHip, LLC**, Austin, TX

Private intellectual property holding company. Purchase and manage a small portfolio of patents.

2003 – Present

Expert Witness

Involved in several cases addressing patent and trade secret infringement in addition to corporate and intellectual property valuation.

Oct 05 – March 08

Senior Vice President of Engineering  
**Keyeye Communications, Inc.**, Sacramento, CA

Managed and built an organization with 50+ team members (Analog, Systems, DSP, Digital, Verification, Physical Design) with an innovative, startup oriented, staffing strategy across several design sites (Sacramento, Minneapolis, India and Australia). The result is industry's lowest power 10GBASE-T single chip product. In addition to the management and the vision, hands-on reasonability for the power architecture, modeling and execution.

Jul 01 – Oct 05

Senior Director of Engineering, Communications Technology Division  
**Xilinx, Inc.**, Austin, TX

Managed an organization with 60+ team members across 4 sites in analog, digital and mixed-signal IC design, modeling, application engineering, systems engineering, product characterization, product engineering, production test engineering, advanced technologies, layout, CAD and information technology.

- Organizational and technical vision for Xilinx's high-speed serial I/O and ASSP technologies (180nm, 130nm, 90nm, 65nm and 45nm generations). This includes contributing to the vision for UXPi which is an industry initiative for evangelizing 10Gbps technology, and the driving of industry standards to support further products.
- Products: Virtex-II PRO X (2 family members), Virtex-4 (5 family members) and RocketPHY (3 non-FPGA family members).
- Technical marketing support for both the platform FPGAs and the ASSPs.
- Customer support and interaction for current and future products.
- Partnership development with several tier 1 and tier 2 companies for process technology, packaging, licensing, high-speed connectors, high-speed backplanes and design. Including establishing industry initiatives at OIF and IEEE committees.
- Involvement in all aspects of the production of IC design including quality assurance and reliability.
- Served on patent committee for the Company.
- Recipient of the innovation of the year award for the Virtex-II Pro X product.

Mar 01 – Jul 01

Co-Founder, President and CEO  
**MadMax Optics, Inc.**, Austin, TX

Co-Founded the company to produce revolutionary simulation software for the optical component industry. Opened the main design center in Hamden, CT. Guided the

company through the seed round financing. This included putting together a 5 year business plan, prospectus and investor presentations.

Aug 98 – Feb 01

Vice President of Wired Products

**RocketChips, INC.**, Austin, TX (Acquired by **Xilinx, Inc.** in Nov 2000)

Contributed to the technical, managerial, organizational and marketing leadership for the company's three design centers in Minneapolis (MN), Ames (IA) and Austin (TX). Directly responsible for approximately 35 employees in Wired.

- Products and IP: SERDES and PCS layers for Gigabit Ethernet (IEEE 802.3z, 802.3ab), 2.5Gbps products for serial backplane applications (including OC-48), 10Gbps (IEEE 802.3ae and OC-192), IEEE 1394 and high-speed high-resolution ADCs and DACs (80Ms/s – 250Ms/s).
- Involved with the company since its inception in January 1997 as an early investor and technical and product development through the Iowa State University research work.
- Managed multi-company and multi-country (Japan, India and US) projects as well as major customers including INTEL, SONY and OKI.

Aug 96 - Jul 98

**Contract IC Designer** (Cellular and wireless ICs - power management)

Mixed-Signal Products Group, **Texas Instruments**, Dallas, TX

Contract design for mixed-signal power management ASICs for cellular applications. Involved in the design, implementation and test of several high volume production integrated circuits (TPS202X, TPS203X, TPS204X, TPS208X and TPS209X).

Jun 95 - Jul 96

**Contract IC Designer** (Analog-to-Digital Converters)

Defense Systems & Electronics Group, **Texas Instruments**, Dallas, TX

Investigation and recommendation of a very high-speed high-resolution pipelined multi-path analog-to-digital converter architecture for communication applications.

Jan 85 - Jul 86

**Software Development Engineer**

Cupertino Integrated Circuits Division, **Hewlett Packard** Company, Santa Clara, CA

Design, implementation and maintenance of circuit design analysis product (HPSPICE).

## ACADEMIC EXPERIENCE

Jul 00 – present

**Collaborating Professor**

Department of Electrical and Computer Engineering

Iowa State University, Ames, Iowa

- Continue to guide MS and PhD graduate students and serve on MS and PhD committees at ISU and at University of Texas, Austin.

Jul 94 – Jul 00

**Associate Professor with Tenure**

Department of Electrical and Computer Engineering

Iowa State University, Ames, Iowa

(On leave of absence from Aug 98-Jul 00. Plus several leaves while consulting for Texas Instruments)

Aug 88 - Jul 94

**Assistant Professor**

Department of Electrical and Computer Engineering

Iowa State University, Ames, Iowa

***Research & Teaching***

Was hired in 1988 by ISU to start the VLSI area in the department. This included establishing research area in VLSI CAD (Symbolic Circuit Analysis, Synthesis Methods for Data Converters) and Analog and Mixed-Signal VLSI (Data Converters, Gigabit speeds Communication Circuits, Magneto-resistive devices).

The largest impact has been the establishment of industrial contacts and the founding of the Analog and Mixed-Signal VLSI Design Center. **The funding commitments on which Dr. Hassoun was a PI or Co-PI have grown to approximately \$4.3 Million by 1998.**

**EDUCATION**

- Jan 86 - Aug 1988 **Ph.D.** in *Electrical Engineering*, **Purdue University**, West Lafayette, IN.  
**Thesis:** *Symbolic Analysis of Large-Scale Networks*  
 - Research Assistant (NSF grant) and a Teaching Assistant (VLSI area).
- Jan 84 - Dec 1984 **M.S.** in *Electrical Engineering*, **Purdue University**, West Lafayette, IN.  
**Thesis:** *A Study of a Semi-Direct Method for Computer Analysis of Large-Scale Circuits*  
 - Research Assistant (IBM grant).
- Aug 80 -Dec 1983 **B.S.** in *Electrical Engineering*, **South Dakota State University**, Brookings, SD.  
 - Teaching assistant during senior year.

**PATENTS**

15 patents granted and 7 pending in the areas of multi-gigabit serial transceivers, high-speed high-resolution ADCs and DACs, Magnetic RAMs, RFID, DSP filters and Power Management.

**Granted:**

1. Richard Willham, Robert Weber, Marwan Hassoun, "Livestock Record System," U. S. Patent No. **5,322,034**, June 21, 1994.
2. Richard Willham, Robert Weber, Marwan Hassoun, "Individual Descriptive Record System," U. S. Patent No. **5,499,626**, March 19, 1996.
3. Roy Hastings, Marwan Hassoun, Neil Gibson, "Capacity Addition Switch Mode Power Converter and Its Controlling Method," **JP2000122737-A**, April 28, 2000.
4. Roy Hastings, Marwan Hassoun, Neil Gibson, Marco Corsi, "Capacitive-summing switch-mode power conversion control," U. S. Patent No. **6,066,943**, May 23, 2000.
5. Roy Hastings, Marwan Hassoun, Neil Gibson, Marco Corsi, "Capacitive-summing switch-mode power conversion control," **EP993104-A3**, December 4, 2000.
6. William Black, Marwan Hassoun, "Non-volatile magnetic circuit," U. S. Patent No. **6,317,359**, November 13, 2001.
7. William Black, Bodhisattva Das, Marwan Hassoun, "Non-volatile spin dependent tunnel junction circuit," U. S. Patent No. **6,343,032**, January 29, 2002.
8. Yvette Lee, Marwan Hassoun, "Segmented DAC calibration circuitry and methodology," U. S. Patent No. **6,489,905**, December 3, 2002.
9. Yvette Lee, Marwan Hassoun, "Current source calibration circuit," U. S. Patent No. **6,507,296**, January 14, 2003.
10. William Black, Bodhisattva Das, Marwan Hassoun, Edward Lee, "Nonvolatile programmable logic devices," U. S. Patent No. **6,542,000**, April 1, 2003.

11. Weibiao Zhang, Marwan Hassoun, "Apparatus for and method of performing a conversion operation," U. S. Patent No. **6,563,444**, May 13, 2003.
12. Justin Gaither, Marwan Hassoun, "Analog Signal Test Circuit and Method", U. S. Patent No. **6,653,827 B2**, November 25, 2003.
13. Ahmed Younis, Marwan Hassoun, "Method and System for VCO-Based Analog-To-Digital Conversion (ADC)," U. S. Patent No. **6,809,676 B1**, October 26, 2004.
14. Moises Robinson, Shahriar Rokhsaz, Marwan Hassoun, Earl Swartzlander, Jr, "Voltage Controlled Oscillator ", U. S. Patent No. **7,315,220**, January 1, 2008.
15. Moises Robinson, Marwan Hassoun, Earl Swartzlander, Jr, "Method and Apparatus for Capacitance Multiplication within a Phase Locked Loop", U. S. Patent No. **7,307,460**, Dec 11, 2007.

### **Pending:**

16. David Tetzlaff, Erich Goetting, Steven Young, Marwan Hassoun, Moises Robinson, "Method and Apparatus for Providing Frequency Synthesis and Phase Alignment in an Integrated Circuit," U. S. Application No. 11/049,329, February 2, 2005.
17. David Tetzlaff, Marwan Hassoun, Steven Anderson, Timothy Hagen, "Adaptive Configuration of Serial Communication Transceiver," U. S. Application No. 11/079,768, March 14, 2005.
18. David Tetzlaff, Marwan Hassoun, "Method and Apparatus for Dynamic Port Provisioning Within A Programmable Logic Device", U. S. Application No. 11/198,576, August 05, 2005.
19. Marwan Hassoun, Moises Robinson, David Tetzlaff, "Method and Apparatus for Redundant Transceiver Architecture," U. S. Application No. 11/435,427, May 16, 2006.
20. Moises Robinson, Marwan Hassoun, Earl Swartzlander, "Method and Apparatus for Capacitance Multiplication within a Phase Locked Loop," International Application No. PCT/US06/464, December 5, 2006.
21. James Little, Marwan Hassoun, David Tetzlaff, Chang-Chi Liu, "Combined method for echo and crosstalk cancellation," U. S. Application, February 7, 2007.
22. "Programmable Link Pulse Shaping for Auto-Negotiation," U. S. Application, February 7, 2007.

### **GRANTS AND CONTRACTS**

- During academic career from 1988 – 1998, secured 25 research grants while at Iowa State University and as part of the Analog and Mixed-Signal VLSI Design Center totaling approximately **\$4.3 Million** from 1988- 1998. The sponsors included: Texas Instruments, Honeywell, Rockwell, RocketChips, Computing Devices International, Control Data Corporation (CDC), Defense Advanced Research Projects Agency (DARPA), National Science Foundation, Carver Trust Foundation, US Department of Education, Center for Non-Destructive Evaluation

1. Co-Principal Investigator (with Black, W., Lee, E. and Geiger, R.), "Mixed-Signal Circuits Laboratory," Carver Trust Foundation, **\$1,000,000** (includes \$500,000 required matching from Iowa State University), August 1998 - July 2000.
2. Principal Investigator (with Geiger, R., Black, W. and Lee, E.), "Analog and Mixed-Signal Center Membership," Texas Instruments, Inc., **\$1,000,000**, Jan 1998 - Dec 2000 (continuation of grant 9).

3. Co-Principal Investigator (with Black, W., Lee, E.K.F. and Geiger, R.), "High Density and Low-energy Magneto-resistive Memory Circuits," Honeywell, Inc. (DARPA), **\$151,091**, Sep 1997 - Dec 1998.
4. Co-Principal Investigator (with Geiger, R., Black, W., Lee, K., Wright, C.), "Restructuring Basic Electronic Circuits Education Around Integrated Circuit Technology of the 1990s," National Science Foundation Instrumentation and Laboratory Infrastructure Program **\$200,000**, Aug 1997 - Jun 1999.
5. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E.), Honeywell, Inc. (DARPA), **\$22,400**, "Testing of Magneto-resistive Structures," Feb 1997 - April 1997 (continuation of grant 8).
6. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E, Bergland, D., Sapatnekar, S., Tridandapani, S. and Weber, R.), "Gigabit Silicon Integrated Circuits," RocketChips, Inc., **\$1,000,000**, Jan 1997 - Dec 2001.
7. Principal Investigator, "Linear IC Product Design", Texas Instruments, Dallas, TX, **\$110,000**, Sep 96 - Aug 97.
8. Co-Principal Investigator (with Black, W., Geiger, R., Lee, E., Honeywell, Inc. (DARPA), **\$100,000**, "Magneto-resistive Memories," May 1996 - April 1997.
9. Co-Principal Investigator (with Geiger, R., Black, W., Hassoun, M., and Lee, E., Texas Instruments, Inc., **\$450,000**, "Analog and Mixed-Signal Center Membership," Jan 1996 - Dec 1998.
10. Principal Investigator (with Geiger, R., Lee, E. and Black, W., Rockwell International Inc., **\$300,000**, "Analog and Mixed-Signal Center Membership," Aug 1996 - Dec 1999.
11. Principal Investigator, "Verification of a Pipeline Analog to Digital Converter for Communication", Texas Instruments, Dallas, TX, **\$10,017**, Jan 96 - Aug 96 (continuation of grant 11).
12. Principal Investigator, "Pipeline Analog to Digital Converter for Communication", Texas Instruments, Dallas, TX, **\$27,755**, Aug 95 - Aug 96.
13. Principal Investigator, "An Investigation of a Pipelined Analog-to-Digital Converter", Texas Instruments, Dallas, TX, **\$37,105**, Jun 95 - Aug 95.
14. Co-Principal Investigator (with Richard Hester), "Low Power Analog-To-Digital Converter", Texas Instruments, Dallas, Texas, **\$27,000**, Aug 93 - May 95.
15. Principal Investigator (with Jim Davis), "High Speed Multi-Protocol ActiveBus Prototype Development," Computing Devices International, Bloomington, Minnesota, **\$2,500**, Aug 93- Dec 93 (continuation of grant 16).
16. Principal Investigator (with Jim Davis), "High Speed Multi-Protocol ActiveBus Prototype Development," Computing Devices International, Bloomington, Minn, **\$15,000**, Aug 92-Aug 93.
17. Co-Principal Investigator (with V. Dalal, S. Burns, H. Hsieh, R. Weber, P. Garikepati), "Graduate Assistance in Microelectronics and Photonics," Department of Education, Washington, D.C., **\$351,000**, Aug 90-Aug 93.
18. Principal Investigator, "Symbolic Analysis of Nonlinear Large-Scale Systems," Engineering Research Institute, Ames, Iowa, **\$3,848**, Oct 92- Jul 93.
19. Faculty Associate (with Charles Wright, Jr.), "A laboratory to Support Computer-Aided Digital Systems Design," National Science Foundation Instrumentation and Laboratory Improvement Program, **\$218,317**, Aug 90-Aug 92.
20. Principal Investigator, "Symbolic Sensitivity Analysis of Large-Scale Circuits," University Research Initiation Grant, Ames, Iowa, **\$6,600**, Jul 91-Jun 92.
21. Principal Investigator, "Symbolic Circuit Simulation in the Time Domain," Engineering

- Research Institute, Ames, Iowa, **\$4,240**, Oct 91- Jun 92.
22. Principal Investigator, "Application of VLSI Circuit Partitioning Technique to Dynamic Clustering of Distributed Multiprocessor Systems," Engineering Research Institute, Ames, Iowa, **\$1,660**, Oct 90-Jun 91.
  23. Co-Principal Investigator (with Art Pohm and Jim Davis), "Design of a New High Speed Serial Bus," Control Data Corporation (CDC), Minneapolis, Minnesota, **\$114,000**, Aug 89-Dec 91.
  24. Principal Investigator, "Investigation Proposal for Hardware Implementation of Non-Destructive Evaluation software," Center for Non-Destructive Evaluation, Ames, Iowa, **\$5,000**, Aug 89-Jun 90.
  25. Principal Investigator, "ASIC Hardware for Image Processing Applications," Engineering Research Institute, Ames, Iowa, **\$4,000**, Oct 89- Jun 90.

### **GRADUATE STUDENTS**

Major Professor for **26 Graduate Students** (8 PhDs and 20 MS (all thesis option)) from 1988 – 2005.

### **TECHNICAL PUBLICATIONS**

Authored or co-authored over 70 technical publications in Technical Journals, Conferences and six chapters of three different books on circuit analysis.

#### **Refereed Journals**

1. Jorgenson, J., Hassoun, M., Hsu, H., "Breakdown Verification for Fault Modeling in Laminate Microstrip Conductors," *International Journal of Microelectronics and Electronic Packaging*.
2. Zhang, R., Hassoun, M., Black, W., Das, B, Wong, K, "Demonstration of a Sensing Four States From A Single Pseudo-Spin Valve GMR Device," *IEEE Transactions on Magnetics*.
3. Shah, J., Younis, A., Sapatnekar, S., Hassoun, M., "A New Method for the Analysis of Power and Ground Busses and its Symbolic Implementation," *IEEE Transactions on Circuits and Systems II*.
4. Hassoun, M. M., Black, W., Lee, K. F., and Geiger, R. L., "Field Programmable Logic Gates Using GMR Devices," *IEEE Transactions on Magnetics*, September 1997.
5. Hassoun, M. M. and Lin, P. M., "A New Method for Symbolic Analysis of Large-Scale Networks," *IEEE Transactions on Circuits and Systems I*, March 1995.
6. Ranmuthu, I., Ranmuthu, K., Pohm, A., Kohl, C., Comstock, C. and Hassoun, M., "A Sensing Scheme for Giant Magneto-Resistive Memories," *IEEE Transactions on Magnetics*, VOL 30, No. 5, September 1994.
7. Hassoun, M. M., Atawale, P., "Hierarchical Symbolic Analysis On A Ncube Multi-Processor," *Alta Frequenza* , (top Italian technical Journal in EE), *invited submission*, VOL 5, No. 6, December 1993, pp. 56-64.
8. Ranmuthu, K., Ranmuthu, I., Pohm, A., Comstock, C. and Hassoun, M., "High Speed (10-20ns) Nonvolatile MRAM with Folded Storage Elements," *IEEE Transactions on Magnetics*, VOL 28, No. 5, September 1992, pp. 2359-2361.

9. Hassoun, M. M. and McCarville, K., "Hierarchical Symbolic Signal-Flow Graph Analysis," *Journal of Analog VLSI and Signal Processing*, Kluwer Publishing, January 1993, pp. 31-42, *invited submission*.
10. Ranmuthu, I., Ranmuthu, K., Kohl, C., Comstock, C. and Hassoun, M., "A 512 Kbit Magneto Resistive Memory with Switched Capacitor Self Referencing Sensing Scheme," *IEEE Transactions on Circuits and Systems II*, VOL. 39, NO. 8, August 1992, pp. 585-587.
11. Ranmuthu, K., Ranmuthu, I., Pohm, A., Comstock, C. and Hassoun, M., "10-35 Nanosecond Magneto-Resistive Memories," *IEEE Transactions on Magnetics*, VOL. 26, No. 5, Sep 1990, pp. 2532-2534.
12. Ranmuthu, I., Ranmuthu, K., Pohm, A., Comstock, C. and Hassoun, M., "Reprogrammable Logic Array Using M-R Elements," *IEEE Transactions on Magnetics*, VOL. 26, No. 5, Sep 1990, pp. 2828-2830.

### Refereed Proceedings Articles

13. Zhang, W., Hassoun, M., "A Redundant-Cell-Relay Continuous Self-Calibration Method for Current-Steering DACs," European Solid-State Circuits Conference, Villach, Austria, September 2001 (accepted for publication).
14. Xia, H., Hassoun, M., "An analog self-calibration algorithm for multibit per stage pipelined Analog to Digital Converters," Proceedings of the *Midwest Symposium on Circuits and Systems*, Dayton, OH, August 2001 (accepted for publication).
15. Chew, S., Hassoun, M., "Implementation, Verification and Synthesis of Gigabit Ethernet 1000BASE-T Physical Coding Sublayer," Proceedings of the *Midwest Symposium on Circuits and Systems*, Dayton, OH, August 2001 (accepted for publication).
16. Liu, H., Hassoun, M., "High Speed Re-Configurable Pipeline ADC Cell Design," *Southwest Symposium on Mixed-Signal Design*, Austin, TX, February 2001.
17. Younis, A., Navin, V., Hassoun, M., "A Calibration Algorithm for a 16-bit Multi-path Pipeline ADC," Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lansing, MI, August 2000.
18. Younis, A., Hassoun, M., "A High Speed Fully differential CMOS Opamp," Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lansing, MI, August 2000.
19. Zhang, W., Hassoun, M., "A Weighted Reduced Connectivity Matrix Partitioning Algorithm," Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lansing, MI, August 2000.
20. Zhang, W., Hassoun, M., "A Small Signal Analysis of a Gain-Boosting Amplifier," *Southwest Symposium on Mixed-Signal Design*, San Diego, CA, February 2000.
21. Liu, H., Hassoun, M., "Components of a 12-bit 50 Ms/s Non-radix 2 Pipeline Analog-to-Digital Converter," Proceedings of the *Midwest Symposium on Circuits and Systems*, East Lansing, MI, August 2000.
22. Xia, H., Bataineh, K., Hassoun, M., Kryzak, J., " An Algorithm for Symbolic and Numeric Architecture Determination in a Knowledge-Based ADC Synthesis Environment using Fuzzy Membership Functions," *IEEE International Symposium on Circuits and Systems*, Orlando, FL, 1999.
23. Xia, H., Bataineh, K., Hassoun, M., Kryzak, J., " A Mixed-signal Behavioral Level Implementation of 1000BASE-X Physical Layer for Gigabit Ethernet," *IEEE International Symposium on Circuits and Systems*, Orlando, FL.

24. Zhang, W., Xia, H., Al-Omari, R., Hassoun, M., "Symbolic Synthesis Of Analog-to-Digital Conversion Architectures Using Direct-Mapping Techniques," *IEEE International Conference on Electronics, Circuits, and Systems*, Lisbon, Portugal, Oct 1998, Invited Paper.
25. Konczykowska, A., Hassoun, M. and Huelsman, L., "Applications Of Symbolic Methods To Circuit Design: An Overview," *IEEE International Symposium on Circuits and Systems*, Monterey, CA, May 1998, accepted for publication.
26. Hassoun, M., and Lin, P-M., "A Formulation Method For Including Ideal Operational Amplifiers In Modified Nodal Analysis," Proceedings of the *Midwest Symposium on Circuits and Systems*, Sacramento, CA, August 1997.
27. Jin, H., Lee, K. F., Hassoun, M., "An Averaging Scheme for multi-path Analog-to-Digital Converters," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Hong Kong, June 1997.
28. Venkata, N., Ray, T., Hassoun, M., Lee, K. F., Black, W., Soenen, E. and Geiger, R. L., "A Simulation Environment for Pipeline Analog-to-Digital Converters," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Hong Kong, June 1997.
29. Hassoun, M. M., Black, W., Lee, K. F., and Geiger, R. L., "Field Programmable Logic Gates Using GMR Devices," Proceedings of the *International Conf on Magnetics*, April 1997.
30. Echtenkamp, J. and Hassoun, M., "Implementation Issues for Symbolic Sensitivity Analysis," Proceedings of the *Midwest Symposium on Circuits and Systems*, Ames, Iowa, August 1996.
31. Hooton, T., O'Farrell, P., Dietrich, W., Salzman, J., Scott, K., Chang, C., Hassoun, M. and Rooks, J., "A 16-bit 25.6 MHz Self-Calibrating Analog-to-Digital Converter," Proceedings of the *Government Microelectronics Applications Conference*, Las Vegas, NV, March 1997.
32. Hassoun, M., Weber, R, Willham, R. and Greenfield, T., "A VLSI Prototype For A Remote Livestock Record System," Proceedings of the *Midwest Symposium on Circuits and Systems*, Rio De Janeiro, Brazil, August 1995.
33. Hassoun, M. and Huelsman, L., "Overview Symbolic Analysis Techniques for Large Analog Integrated Circuits," Proceedings of the *Midwest Symposium on Circuits and Systems*, Rio De Janeiro, Brazil, August 1995.
34. Echtenkamp, J., Hassoun, M., Prabhu, G. and Wright, C., "Symbolic Sensitivity Analysis Method for SCAPP ," 1995 *European Conference on Circuit Theory and Design*, Davos, Switzerland, September 1995, *invited paper* .
35. Hassoun, M. and Huelsman, L., "Overview Symbolic Analysis Techniques for Large Analog Integrated Circuits," *IEEE International Symposium on Circuits and Systems*, Seattle, WA, May 1995, *invited paper* (paper was presented but did not appear in the proceedings due to a clerical error, see R27).
36. McCarville, K., Hassoun, M., "Symbolic Simulation of Semiconductor Devices in SCAPP," Proceedings of the *Midwest Symposium on Circuits and Systems*, Lafayette, LA, August 1994.
37. Hassoun, M., Fernández, F., Gielen, G., Huelsman, L., Konczykowska, A., Manetti, S., Sansen, W. and Vlach, Jiri, "Pleasures, Perils and Pitfalls of Symbolic Analysis," Proceedings of the *IEEE International Symposium on Circuits and Systems*, London, England, June 1994, pp. 1.451-1.457.
38. Greenfield, S., Hassoun, M., "Direct Symbolic Transient Analysis Using Approximate Integration Formulae," Proceedings of the *IEEE International Symposium on Circuits and Systems*, London, England, June 1994, pp. 1.29-1.36.
39. Alspaugh, B., Hassoun, M., "A Mixed Symbolic and Numeric Method for Closed-Form Transient Analysis ," 1993 *European Conference on Circuit Theory and Design*, Davos,

- Switzerland, September 1993, pp. 1687-1692, *invited paper*.
40. Hassoun, M., Atawale, P., "Symbolic Analysis of Large-Scale Network on Multi-Processor Systems," 1993 *IEEE International Symposium on Circuits and Systems*, Chicago, May 1993, pp. 1651-1654.
  41. Sandage, R., Sancheti, P., Hassoun, M., Weber, R., Stephenson, D., "A 2 $\mu$  Analog CMOS Implementation Of An Aircraft Communication Monitor," Proceedings of the 1992 Midwest Symposium on Circuits and Systems, Washington D.C., August 1992, pp. 1081-1084.
  42. Ng, S., Van Peurse, J., Hassoun, M., Davis, J., Pohm, A., "A VLSI Implementation Of An Interface For A Dual Protocol High Speed Active Bus," Proceedings of the 1992 Midwest Symposium on Circuits and Systems, Washington D.C., August 1992, pp. 1077-1080.
  43. Ranmuthu, I., Ranmuthu, K. T., Kohl, C., Comstock, C., Hassoun, M., "A CMOS Process Compatible High Density Magneto-Resistive Memory," Proceedings of the 1992 Midwest Symposium on Circuits and Systems, Washington D.C., August 1992, pp. 307-309.
  44. Ranmuthu, I., Ranmuthu, K. T., Comstock, C., Hassoun, M., "Magneto-Resistive Memories- An Alternative for Floating Gate Technology," Proceedings of the 1992 Midwest Symposium on Circuits and Systems, Washington D.C., August 1992, pp. 134-136.
  45. Hassoun, M. M., Alspaugh, B., and Burns, S., "A State-Variable Approach to Symbolic Circuit Simulation in The Time Domain," Proceedings of the *IEEE International Symposium on Circuits and Systems*, San Diego, CA, May 1992, pp. 682-685, *invited paper*.
  46. Ranmuthu, I., Ranmuthu, K., Pohm, A., Kohl, C., Comstock, C. and Hassoun, M., "A Sensing Scheme for Giant Magneto-Resistive Memories," Proceedings of the *International Conference on Magnetism*, April 1994.
  47. Ranmuthu, K., Ranmuthu, I., Pohm, A., Comstock, C. and Hassoun, M., "High Speed (10-20ns) Nonvolatile MRAM with Folded Storage Elements," Proceedings of the *International Conference on Magnetism*, April 1992.
  48. Hassoun, M. M., Smay, T. A., Wright, C. T., and Irwin, S. A., "A VLSI Design, Testing, and Interfacing Experiment," Proceedings of the 1991 *Microelectronics Education Conference and Exposition*, San Jose, California, August 1991, pp 23-33.
  49. Hassoun, M. M., "Design, Implementation and Evaluation of a VLSI High Speed Array Processor for real-Image Processing Morphology Operations," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Singapore, June 1991, pp. 2363-2366.
  50. Hassoun, M. M., "Hierarchical Symbolic Analysis of Large-Scale Systems Using A Mason's Signal Flow Graph Model," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Singapore, June 1991, pp. 809-812, *invited paper*.
  51. Hassoun, M. M. and Gosti, W., "Block Partitioning of VLSI Circuits Using a Reduced Information Set Matrix," Proc. of the *IEEE International Symposium on Circuits and Systems*, Singapore, June 1991, pp. 2040-2043.
  52. Hassoun, M. M. and Ackerman J. E., "Symbolic Simulation of Large-Scale Circuits in Both Frequency and Time Domains," Proceedings of the 33rd *IEEE Midwest Symposium on Circuits and Systems*, Calgary, Alberta, August 1990, pp. 707-710.
  53. Hassoun, M. M., Smay, T. A., Wright, C. T., and Irwin, S. A., "The VLSI Program at Iowa State University," Proceedings of the 1990 *Microelectronics Education Conference and Exposition*, San Jose, California, August 1990, pp. 207-218.
  54. Hassoun, M. M. and Lin, P. M., "An Efficient Partitioning Algorithm for Large-Scale Circuits," Proceedings of the *IEEE International Symposium on Circuits and Systems*, New Orleans, Louisiana, May 1990, pp. 2405-2408.
  55. Lin, P. M. and Hassoun, M. M., " More General Characterization of Linear N-Terminal Components for Large-Scale Networks," Proceedings of the *IEEE International Symposium*

- on Circuits and Systems*, New Orleans, Louisiana, May 1990, pp. 2413-2416.
56. Ranmuthu, K., Ranmuthu, I., Pohm, A., Comstock, C. and Hassoun, M., "10-35 Nanosecond Magneto-Resistive Memories," Proceedings of the *International Conference on Magnetism*, April 1990.
  57. Ranmuthu, I., Ranmuthu, K., Pohm, A., Comstock, C. and Hassoun, M., "Reprogrammable Logic Array Using M-R Elements," Proceedings of the *International Conference on Magnetism*, April 1990.
  58. Hassoun, M. M. and Lin, P. M., "An Efficient Network Approach to Symbolic Simulation of Large-Scale Circuits," Proceedings of the *IEEE International Symposium on Circuits and Systems*, Portland, Oregon, May 1989, pp. 806-809, *invited paper*.
  59. Hassoun, M. M. and Lin, P. M., "Performance Analysis of a Relaxation Method for Simulation of Large-Scale Circuits," Proceedings of the *IEEE International Symposium on Circuits and Systems*, San Francisco, California, May 1985, pp. 711-714.

### Non-Referred Proceeding Articles

60. Shah, J., Sapatnekar, S., Hassoun, M., "Application of Symbolic Analysis to Power and Ground Interconnect Optimization," Proceedings of the 1996 *International Workshop on Symbolic Methods and Applications to Circuit Design*, Leuven, Belgium, Oct 1996, *invited contribution*.
61. Jacobson, D., Reddy, S., Hassoun, M., Kuhl, J., and Jones, E., "A Course Exchange Using Television," Proceeding of the 1994 Frontiers in Education Conference, San Jose, CA, November 1994, pp. 586-588.
62. Hassoun, M. , Echtenkamp, J., "Symbolic Sensitivity Analysis for Sequence of Expression Methods," Proceedings of the 1994 *International Workshop on Symbolic Methods and Applications to Circuit Design*, Seville, Spain, Oct 1994, pp. 115-132, *invited contribution*.
63. Freeman, P., Hassoun, M., "A Color Substitution Controller for the IBM-PC," *1993 Electro-technology Conference* , Ames, Iowa, April 1993, pp. 18-21.
64. Hassoun, M. , Atawale, P., "Symbolic Analysis On A nCUBE Multi-Processor Machine," Proceedings of the 1992 *International Workshop on Symbolic Methods and Applications to Circuit Design*, Florence, Italy, Oct 1992, pp. 185-198, *invited contribution*.
65. Kohl, C., Jano, B., Hassoun, M., "Dynamic Compression/Decompression 2 $\mu$ m CMOS Chip." Proceedings of the 1992 Midwest Electro-Technology Conf, Apr 1992, pp. 31-34.
66. Van Peurseem, J., Ng, S., Hassoun, M., Davis, J., Pohm, A., "A VLSI Design and Implementation of a High Speed Active Backplane Bus Interface Unit." Proceedings of the 1992 Midwest Electro-Technology Conference, April 1992, pp. 31-34.
67. Hassoun, M., Meyer T., Sequiera P., Basart J., " A VLSI Gray-Scale Morphology Processor for Real-Time NDE Image Processing Applications," Proc. of the *SPIE Inter. Society for Optical Engineering Image Algebra and Morphological Image Processing*, San Diego, California, July 1990, pp. 370-379.
68. Hassoun, M. M., " Symbolic Circuit Simulation in the Time Domain," Proceedings of the 1991 *International Workshop on Symbolic Methods and Their Applications to Circuit Design*, French Centre National d'Etudes des Telecommunications, Paris, France, October 1991, pp. 4.1.1-4.1.16, *invited contribution*.
69. Gutierrez, A. and Hassoun, M., "Pipelined IEEE 754 32-bit Floating Point Multiplier," Proceedings of the *Design Technology Conference*, May 1988, pp. 4.6.1 - 4.6.8.
70. Dowell, R., Hassoun, M. and Luo, R., "HPSPICE, a Hierarchical Design," Proceedings of the *Design Technology Conference*, May 1986, pp. S3.5.1-S3.5.9.

## **Books or Chapters of Books**

1. Hassoun, M., Analog CAD Tools: Symbolic Techniques And Applications, Two Chapters:
  - 1) "Introduction to Symbolic Analysis Methods,"
  - 2) "Hierarchical Symbolic Analysis of Large-Scale Circuits."

**Editors:** A. Rodríguez-Vázquez, F. Fernández & J. Huertas.  
**Publisher:** *IEEE Press*, 1998.
2. Hassoun, M., The Circuits and Filters Handbook, Chapter entitled: "Symbolic Network Analysis."  
**Editors:** Wai-Kai Chen  
**Publisher:** *CRC Press*, 1995.
2. Hassoun, M., The Circuits and Filters Handbook, Two Chapter entitled: "Symbolic Analysis." and "Symbolic Analysis Methods"  
**Editors:** Wai-Kai Chen  
**Publisher:** *CRC Press*, 2002.

## **INVITED TECHNICAL PRESENTATIONS**

Over 40 technical presentations at various companies, conferences and workshops. Latest was an invited presentation at the 2006 ICCAD (International Conference on Computer-Aided Design). Topic: "**Integrated High-Performance Analog and Mixed-Signal – What is the Optimal Process Technology to Use?**"

## **HONORS AND AWARDS**

2004	<u>Recipient:</u> Distinguished Engineer Award, South Dakota State University
2003	<u>Recipient:</u> Innovation of the year award, Xilinx, Inc.
1998	<u>Nominee:</u> Iowa State University Faculty of the Year award
1996	<u>Inductee:</u> Senior member Institute of Electrical and Electronics Engineers (IEEE)
1996	<u>Recipient:</u> Warren Bost Teaching Award Department of Electrical and Computer Engineering, ISU
1993	<u>Nominee:</u> ISU Foundation Early Teaching Achievement Award (only one nomination per department)
1992	<u>Nominee:</u> ISU Foundation Early Teaching Achievement Award (only one nomination per department)
1982	<u>Inductee:</u> Eta Kappa Nu (Electrical Engineering Honor Society) <u>Inductee:</u> Tau Beta Pi (Engineering Honor Society) <u>Inductee:</u> Phi Kappa Phi (National Honor Society)
1980	<u>Inductee:</u> Alpha Lambda Delta (Freshman Honor Society)

## **PROFESSIONAL ACTIVITIES**

*Standards* – Participant and voter on IEEE 802 Standards Committee, in particular on the 802.3 group.

*Conferences & Workshops* – Served as conference chair, on technical program committees, on organizing committees, publicity chair, special sessions chair and steering committees for more than 20 occasions covering more than 7 conferences and workshops.

*Reviewer* – Editor and Referee for IEEE, IEE and other journals in the area of VLSI and circuits and systems.

### ***Conference Organizing Committees***

- 1998 *IEEE International Symposium on Circuits and Systems*, Organizer of a Special Session on Symbolic Analysis, Monterey, CA, May 1998.
- 1998 *Great Lakes Symposium on VLSI*, **Student Paper Judge**.
- 1998 *Great Lakes Symposium on VLSI*, **Industrial Liaison**.
- 1995-present *Midwest Symposium on Circuits on Systems* **Steering Committee**.
- 1994-present *International Workshop on Symbolic Methods and Their Applications to Circuit Design* **Steering Committee**.
- 1996 *Midwest Symposium on Circuits on Systems*, **General Chairperson**.  
The conference had approximately 300 papers in it, six parallel sessions, 5 tutorial sessions and several plenary speakers. Dr. Hassoun was responsible for 90% of the planning and organization of the conference.
- 1996 *Great Lakes Symposium on VLSI*, **Publicity Chairperson**.
- 1996 *International Workshop on Symbolic Methods and Their Applications to Circuit Design*, **Workshop Organizing Committee**.
- 1996 *IEEE International Symposium on Circuits and Systems*, Organizer of a Special Session on Symbolic Analysis, Atlanta, GA, May 1996.
- 1995 *European Conference on Circuit Theory and Design*, Organizer of a Special Session on Symbolic Analysis, Istanbul, Turkey, August 1995.
- 1995 *IEEE International Symposium on Circuits and Systems*, Organizer of a Special Session on Symbolic Analysis, Seattle, WA, May 1995.
- 1994 *IEEE International Symposium on Circuits and Systems*, Organizer of a Panel Session on "Symbolic Circuit Analysis Methods And Their Application To Circuit Design," London, England. June 1994
- 1994 *Electro-Technology Conference*, Ames, Iowa, April 1993.
- 1993 *Electro-Technology Conference*, Ames, Iowa, April 1993.
- 1992 *IEEE International Symposium on Circuits and Systems*, Organizer of a Special Session on "Theory and Application of Symbolic Circuit Analysis," San Diego, CA, May 1992.
- 1992 *Electro-Technology Conference*, Ames, Iowa, April 1992.

### ***Conferences and Workshops Session Chair & Moderator***

- 2000 *IEEE International Symposium on Circuits and Systems*, **Session Chair** for a Special Session on Symbolic Analysis, Switzerland, June 2000.
- 1998 *IEEE International Symposium on Circuits and Systems*, **Session Chair** for a Special Session on Symbolic Analysis, Monterey, CA, May 1998.
- 1996 *International Workshop on Symbolic Methods and Applications to Circuit Design*, **Session**

- Chair**, Leuven, Belgium, October 1996.
- 1996 *International Workshop on Symbolic Methods and Applications to Circuit Design*, **Panel Session**, Leuven, Belgium, October 1996.
- 1996 *IEEE International Symposium on Circuits and Systems*, **Session Chair** for a Special Session on Symbolic Analysis, Atlanta, GA, May 1996.
- 1995 *IEEE International Symposium on Circuits and Systems*, **Session Chair** for a Special Session on Symbolic Analysis, Seattle, WA, May 1995.
- 1994 *International Workshop on Symbolic Methods and Applications to Circuit Design*, **Panel Session Moderator**, Seville, Spain, October 1994.
- 1994 *International Workshop on Symbolic Methods and Applications to Circuit Design*, **Session Chair**, Seville, Spain, October 1994.
- 1994 *IEEE International Symp on Circuits and Systems*, **Panel Session Moderator** on "Symbolic Circuit Analysis Methods And Their Application To Circuit Design," London, England. June 1994.
- 1992 *International Workshop on Symbolic Methods and Applications to Circuit Design*, **Session Chair**, Florence, Italy, October 1992.
- 1992 *IEEE International Symposium on Circuits and Systems*, **Session Chair** for a Special Session on "Theory and Application of Symbolic Circuit Analysis," San Diego, CA, May 1992.
- 1992 *Electro-Technology Conference*, **Session Chair** for Computer Engineering Sessions, Ames, Iowa, April 1992.
- 1991 *International Workshop on Symbolic Methods and Their Applications to Circuit Design*, **Session Chair**, Paris, France, Oct 1991.

### Professional Societies

- 1996-present **Senior Member** Institute of Electrical & Electronics Engineers
- 1982-present **Member** Institute of Electrical & Electronics Engineers
- 1984-present **Member** Circuits and Systems Society of IEEE
- 1996-present **Member** Solid-State Circuits Society of IEEE
- 1991-present **Member** American Society of Engineering Education

### Reviewer

Guest Editor: IEEE Transactions on Circuits and Systems II, Special Issue on Symbolic Analysis 1998.

### New Text Book Review:

Authors: Steve Kang & Yousef Leblebici, University of Illinois Urbana-Champaign  
 Title: "CMOS Digital Integrated Circuits" Publisher: McGraw Hill, New York, NY.

Referee, IEE Electronic Letters, United Kingdom.

Referee, International Journal Circuit Theory and Applications.

Referee, IEEE Transactions on Circuits and Systems.

Referee, IEE Proceedings (Institute of Electrical Engineers, United Kingdom).

Referee, Alta Frequenza (top Italian technical Journal in EE).

Reviewer, 1993 and 1995 European Conference on Circuit Theory and Design.

Reviewer, 1994, 1995, 1996 and 1997 IEEE Midwest Symposium on Circuits and Systems.

Reviewer, 1992, 1994, 1995, 1996 and 1997 IEEE International Symposium on Circuits and Systems.

Referee, IEEE Transactions on Education.

Reviewer, National Science Foundation, Directorate for Computer and Information Science and Engineering, Division of Microelectronics Information Processing Systems.

**References:**

- Supplied upon request.